Figure 1

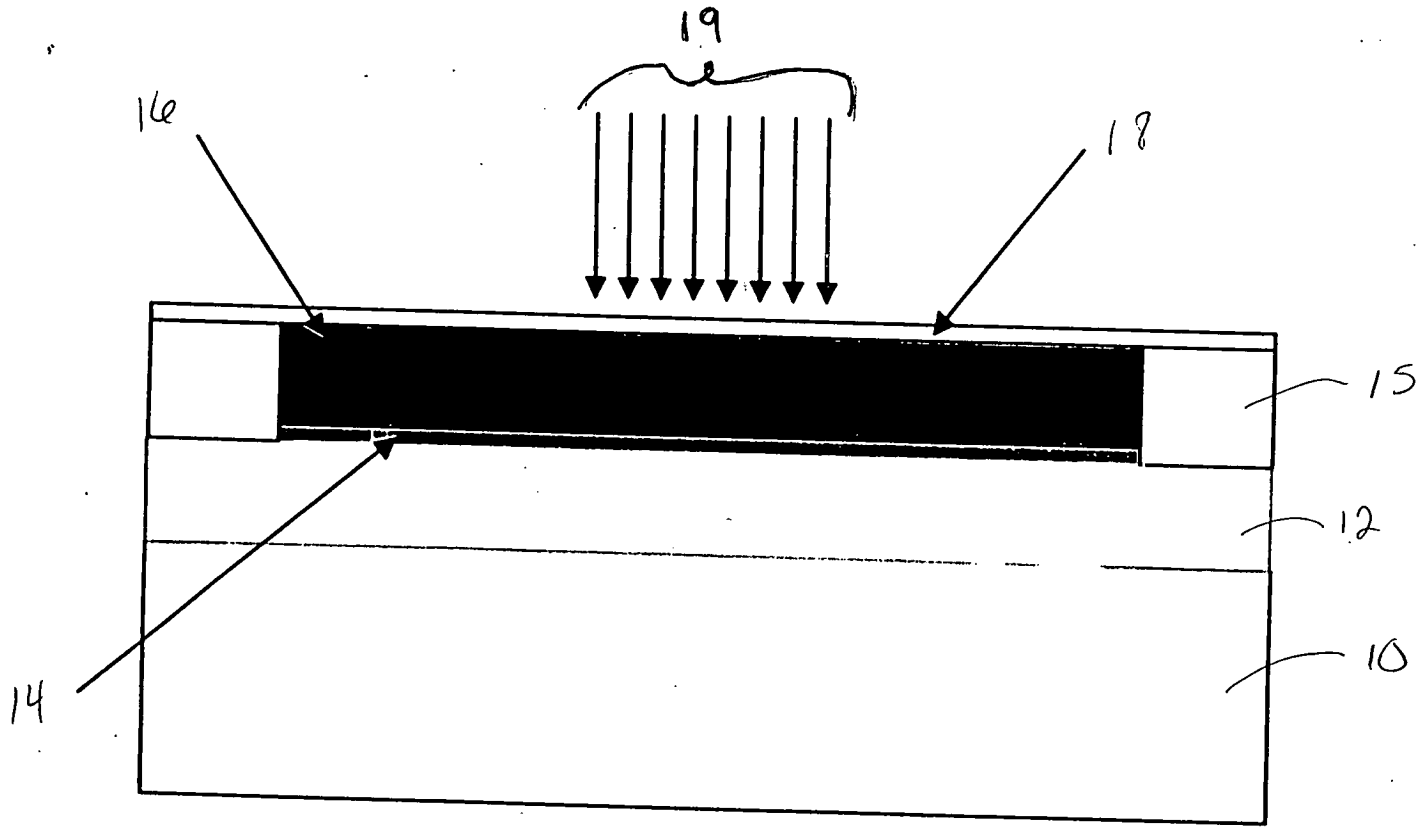


Figure 2

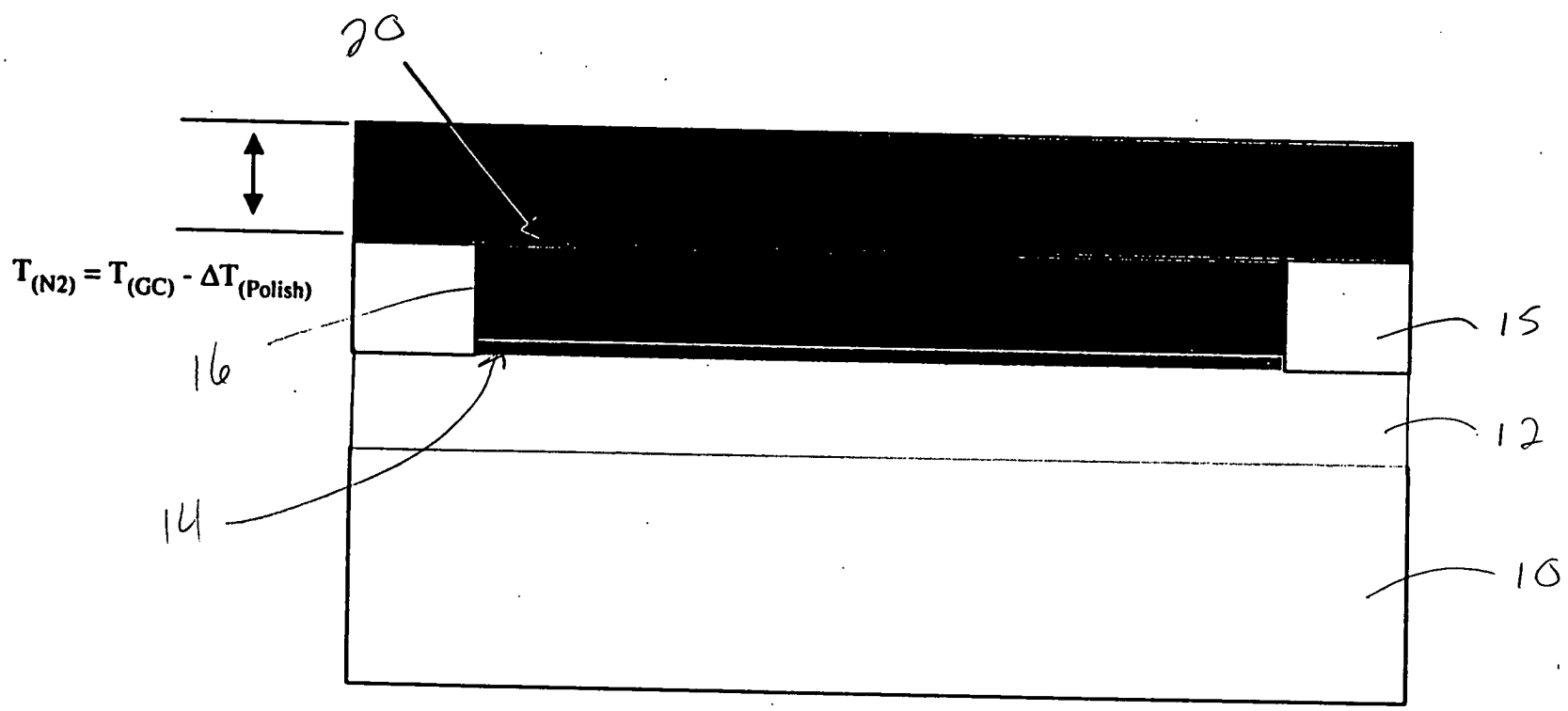


Figure 3

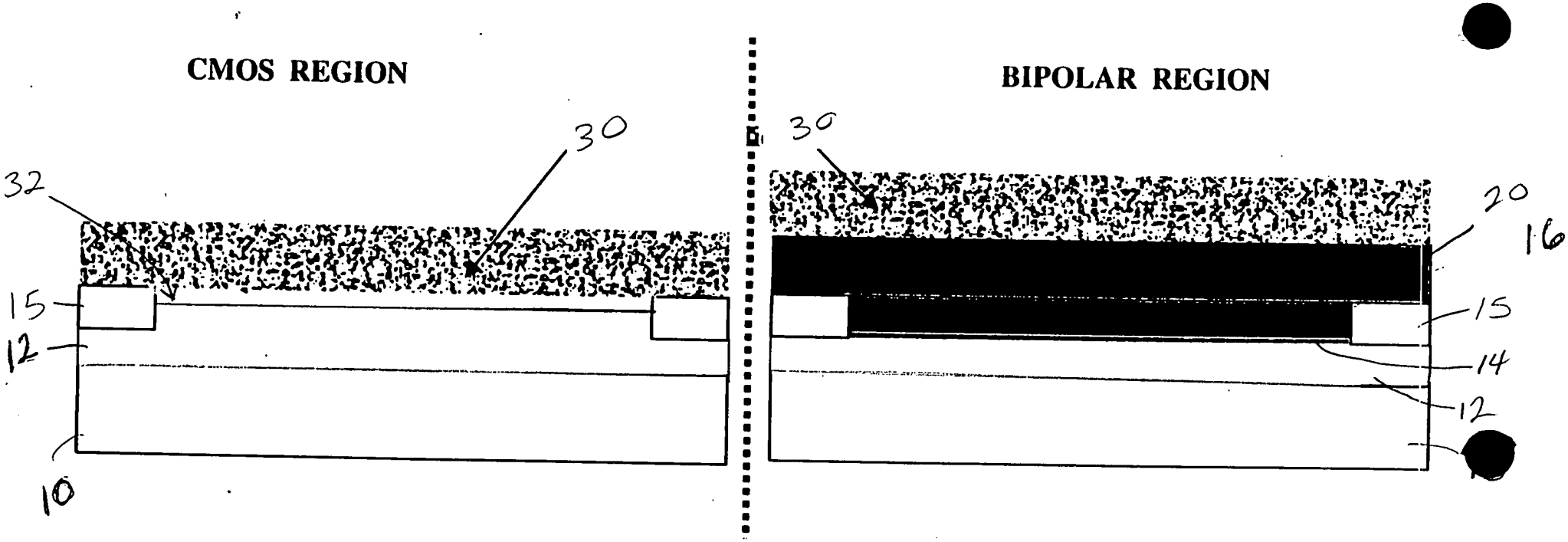


Figure 4

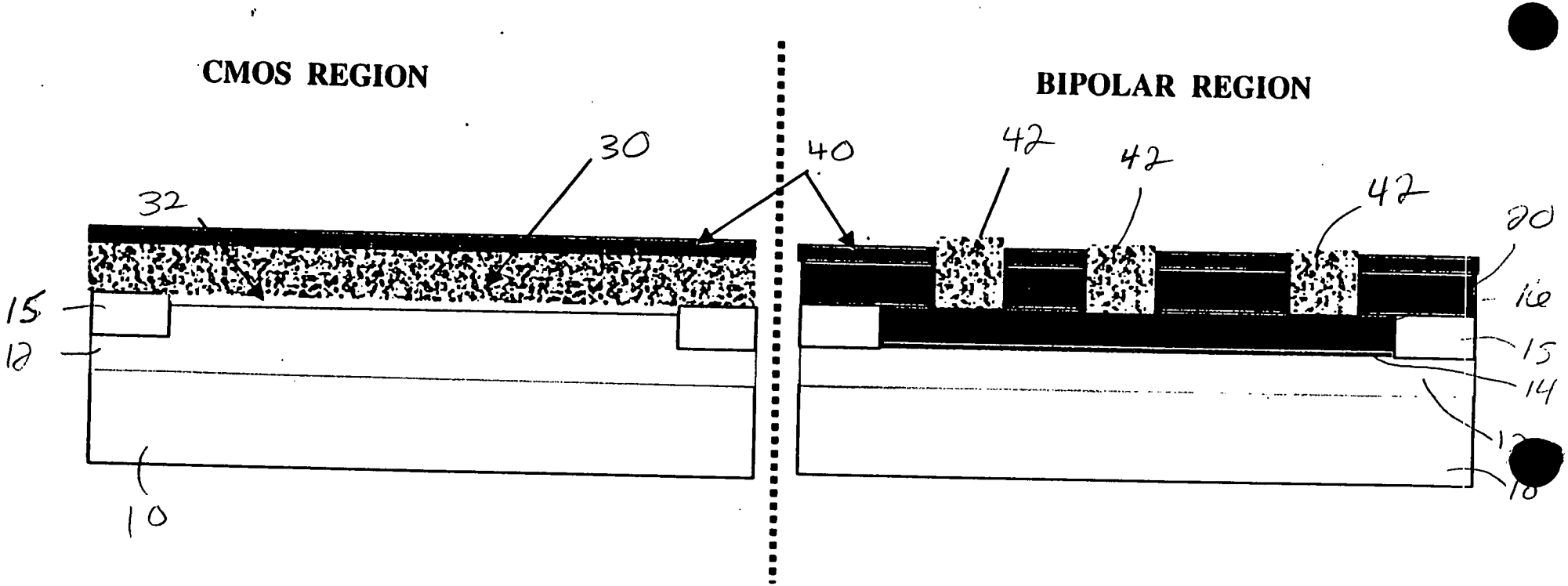

CMOS REGION
BIPOLAR REGION
30
40
42
42
42
32
20
16
15
12
15
14
10
10

Figure 5

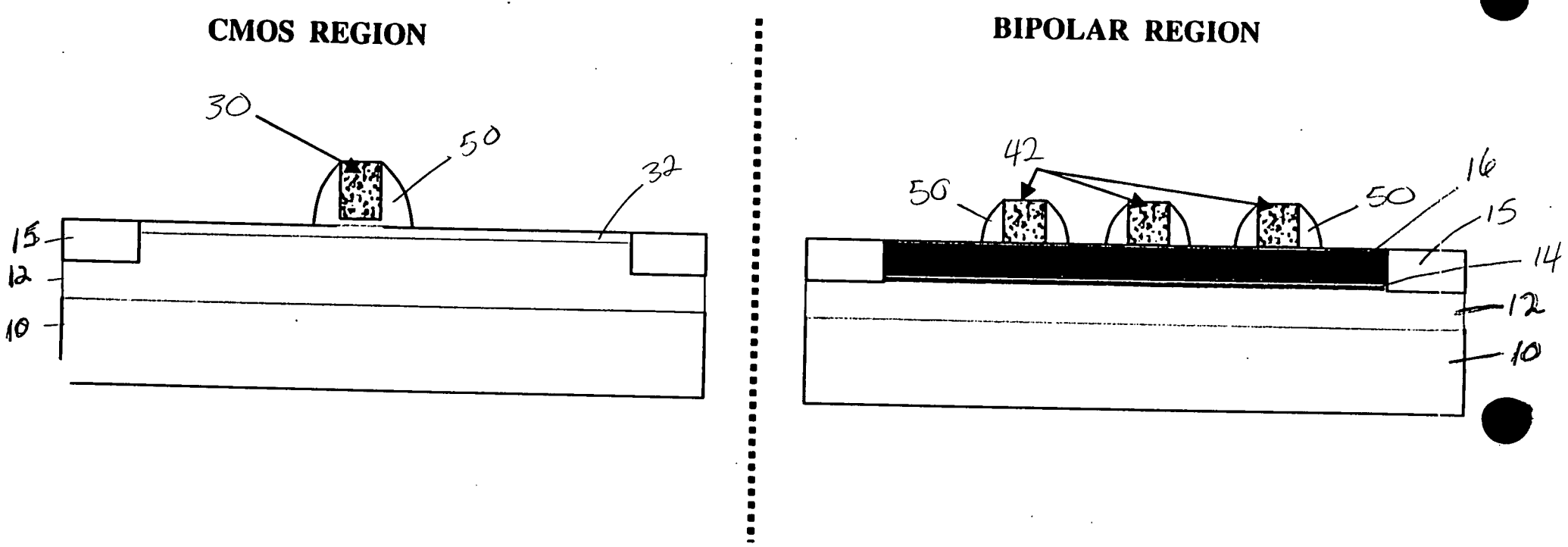

CMOS REGION
BIPOLAR REGION
30
50
32
15
12
10
42
50
50
16
15
14
12
10

Figure 6

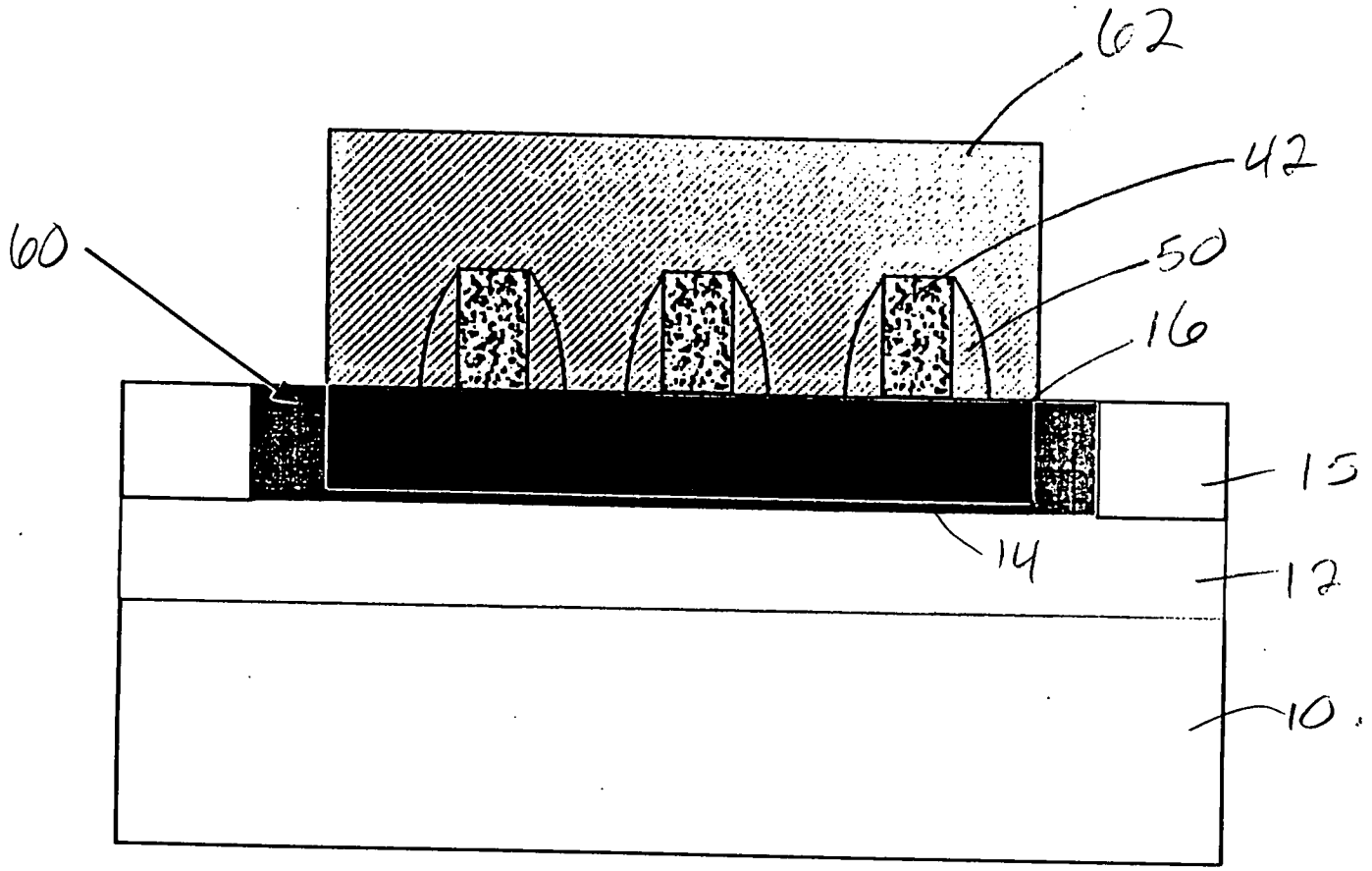


Figure 7

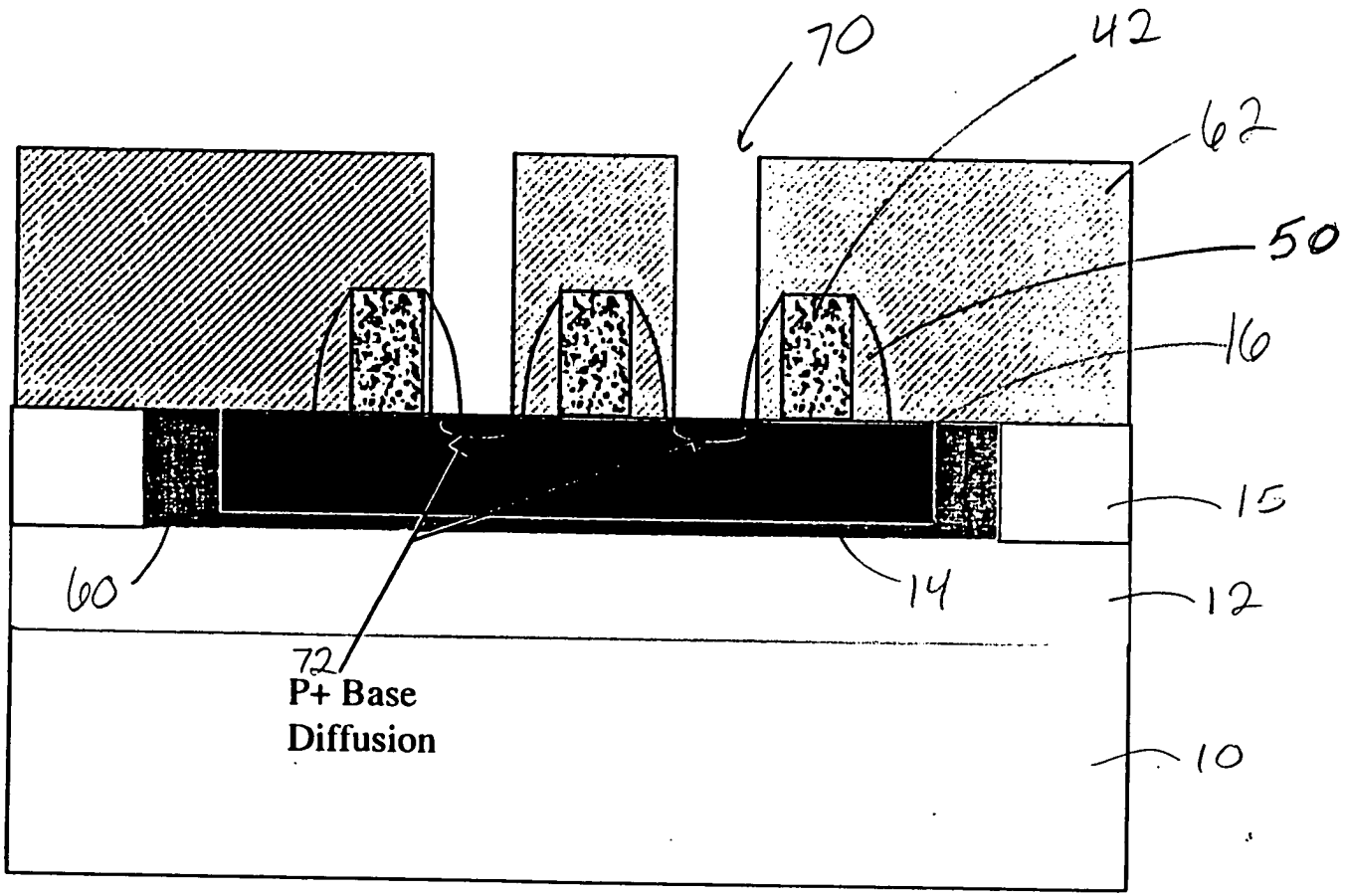


Figure 8

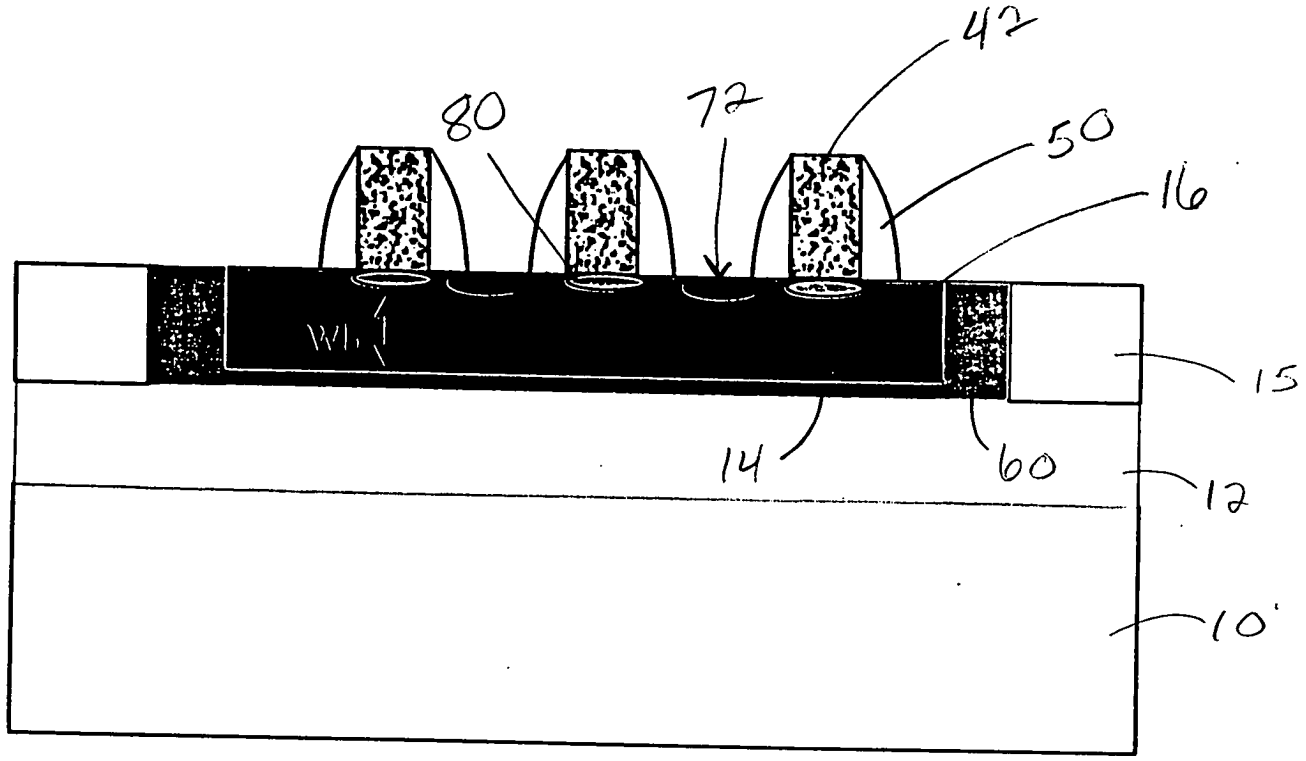
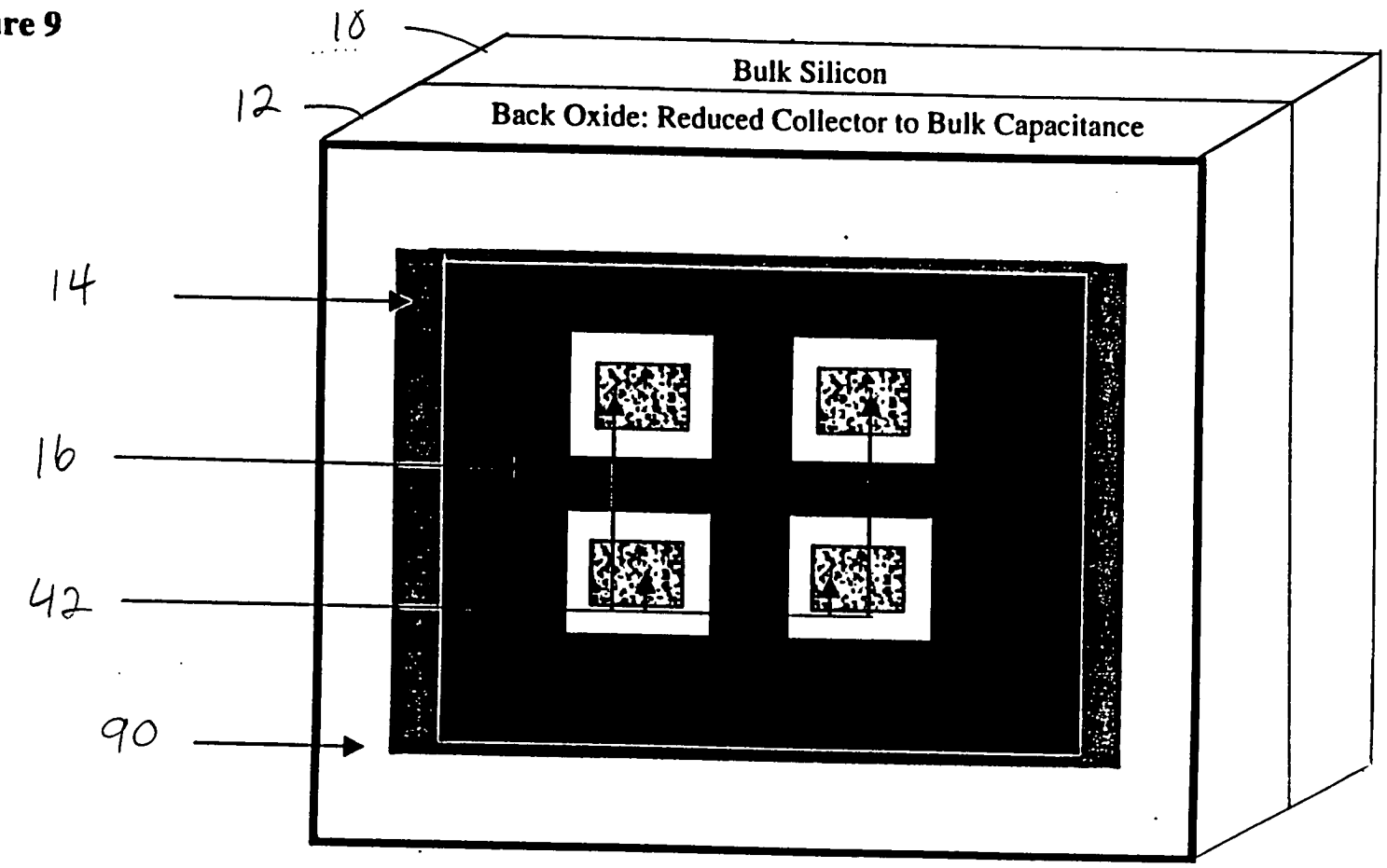


Figure 9


10
12
Bulk Silicon
Back Oxide: Reduced Collector to Bulk Capacitance
14
16
42
90

Collector Doping Profile

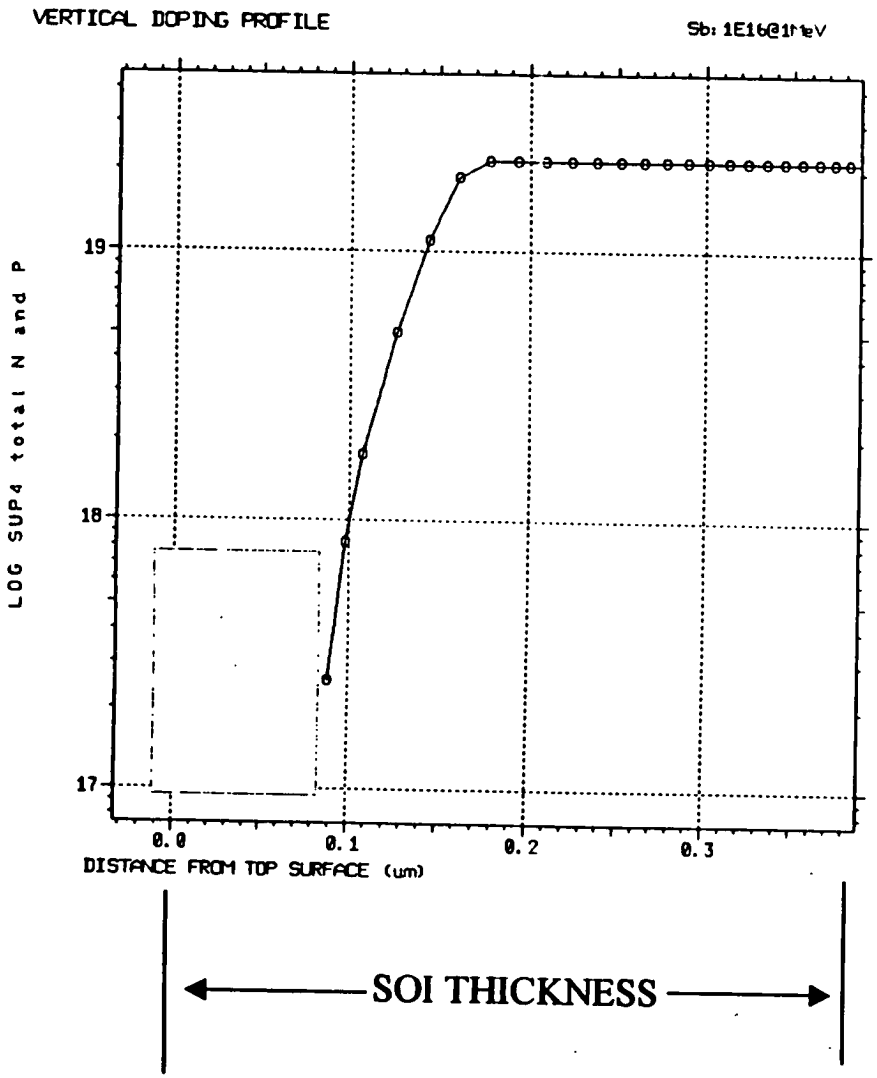


Figure 16A

D.C. Beta vs. Vbe

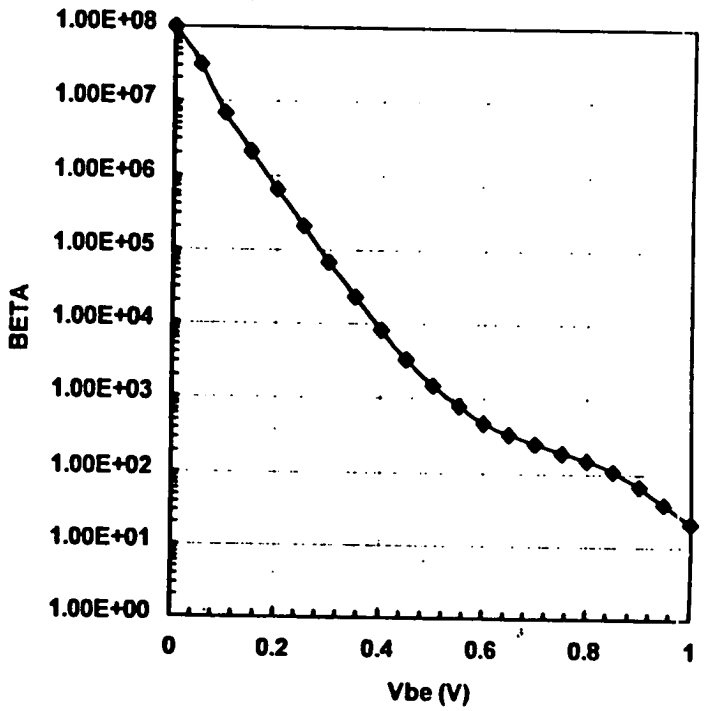


Figure 16B

Figure 11

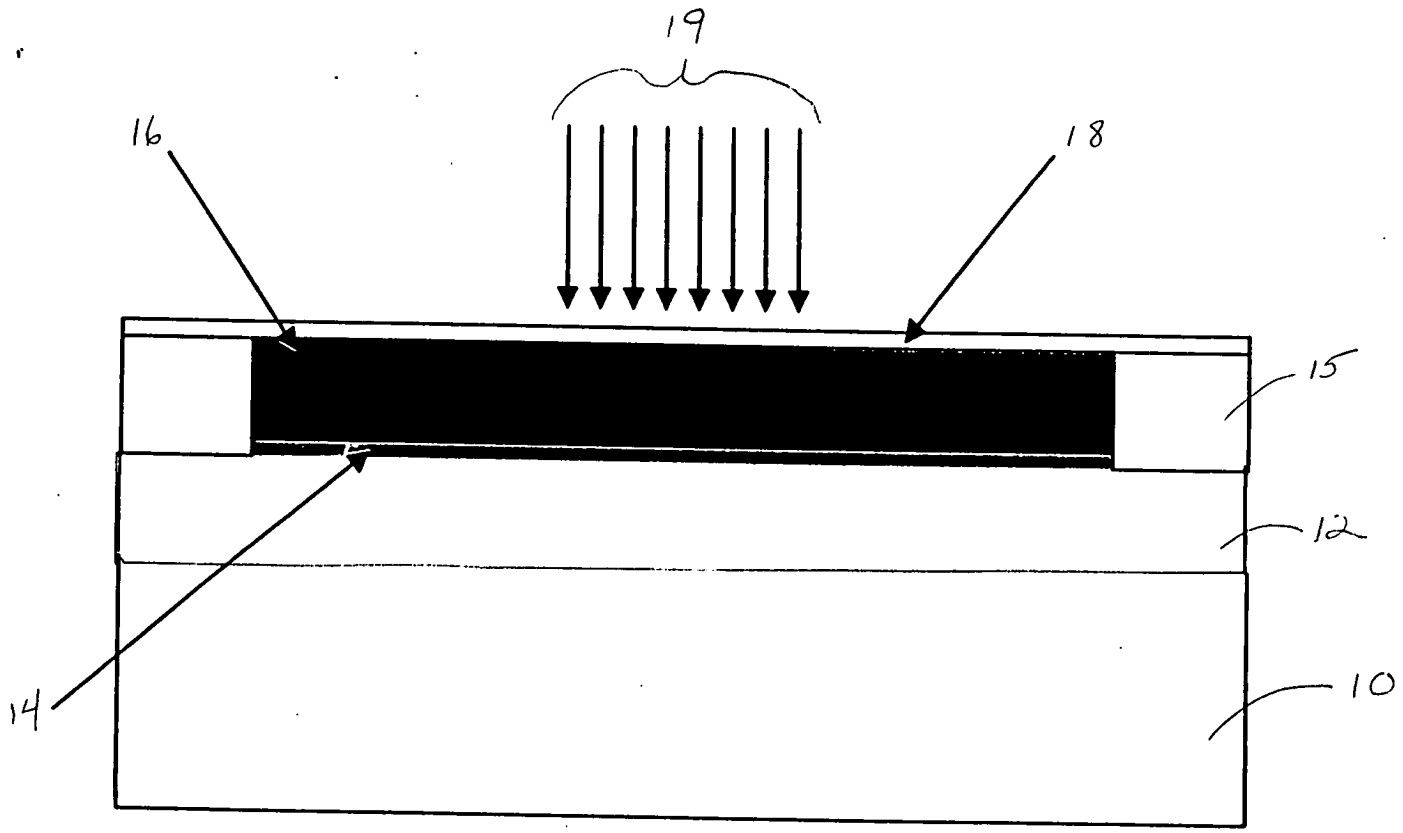


Figure 12

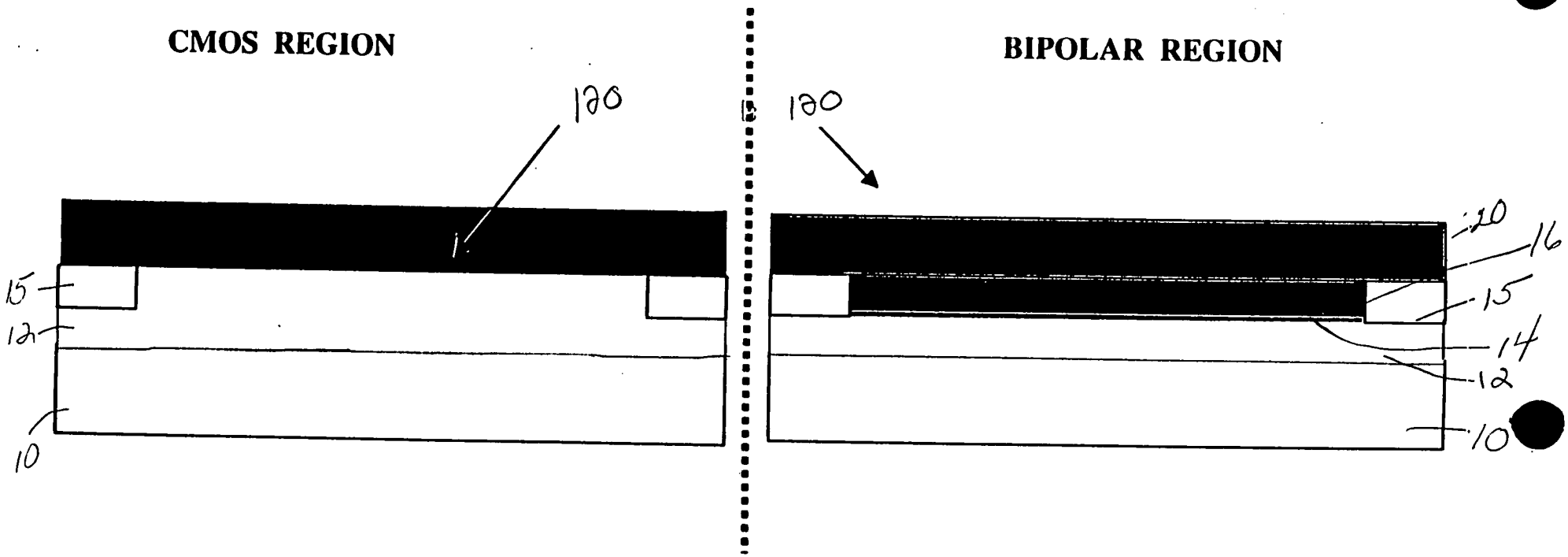


Figure 13

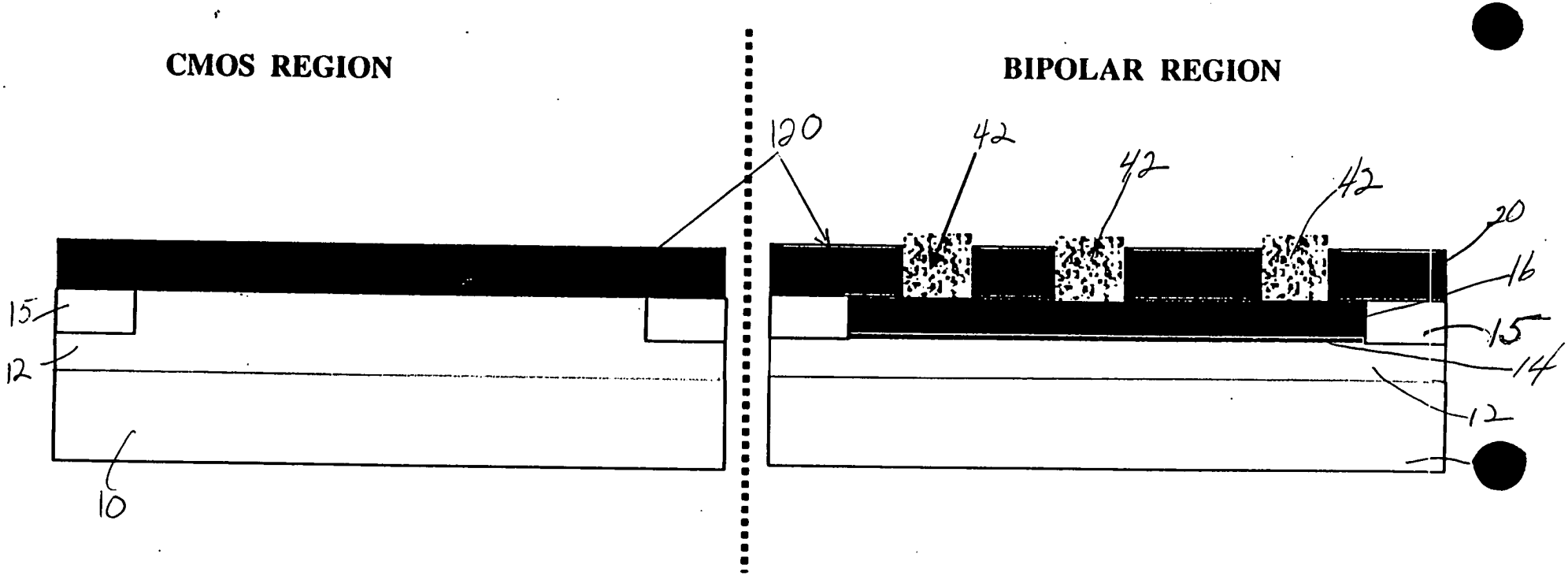


Figure 14

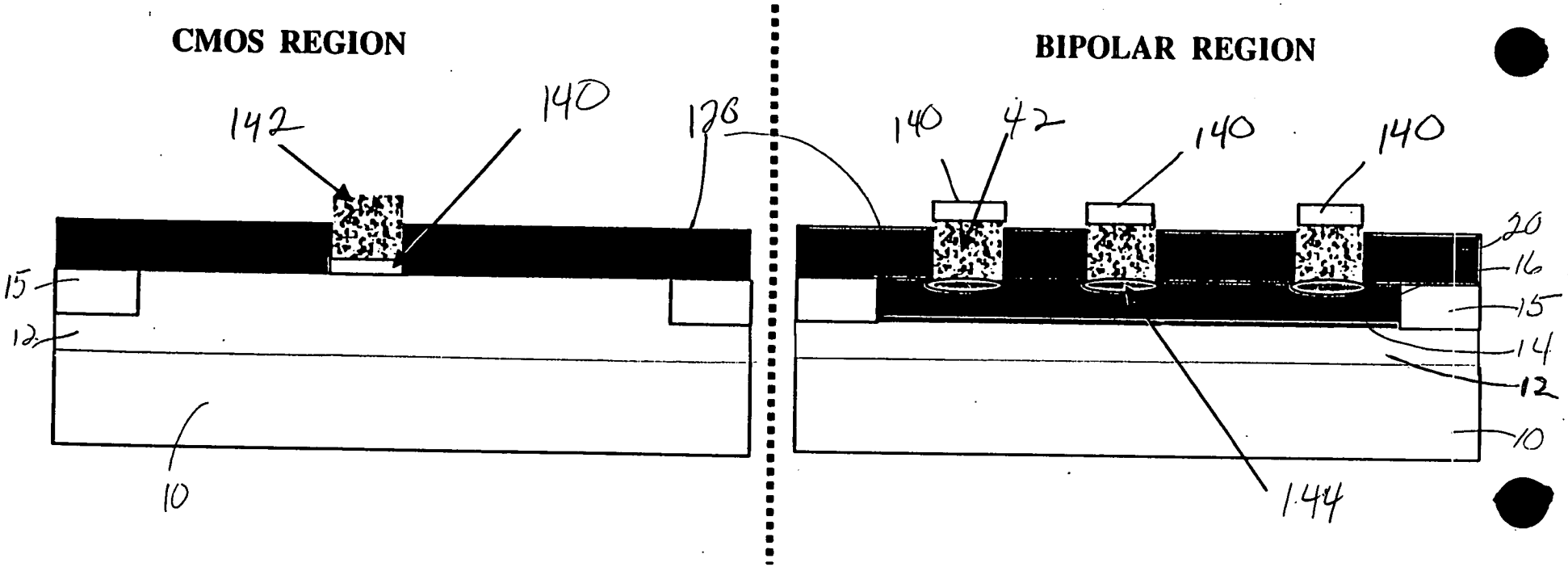

CMOS REGION
BIPOLAR REGION
142
140
126
140
42
140
140
20
16
15
14
12
10
15
12
10
144

Figure 15:

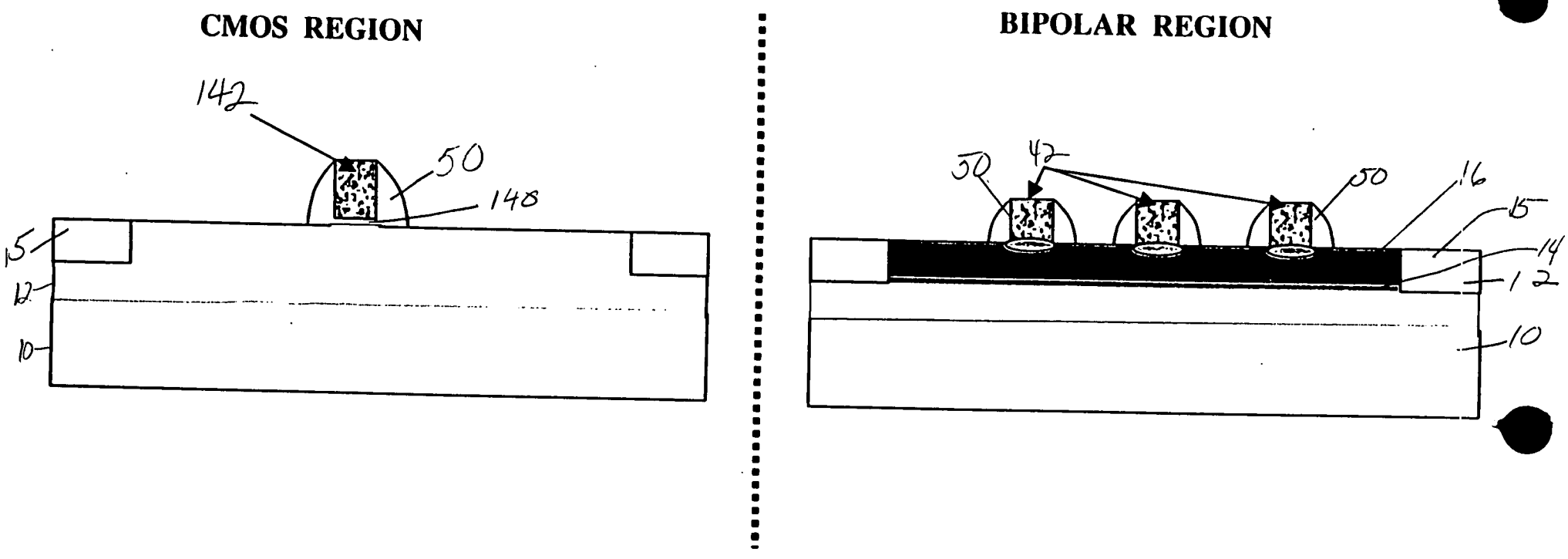

CMOS REGION
142
50
140
15
12
10
BIPOLAR REGION
50
42
50
16
15
14
12
10

Figure 16

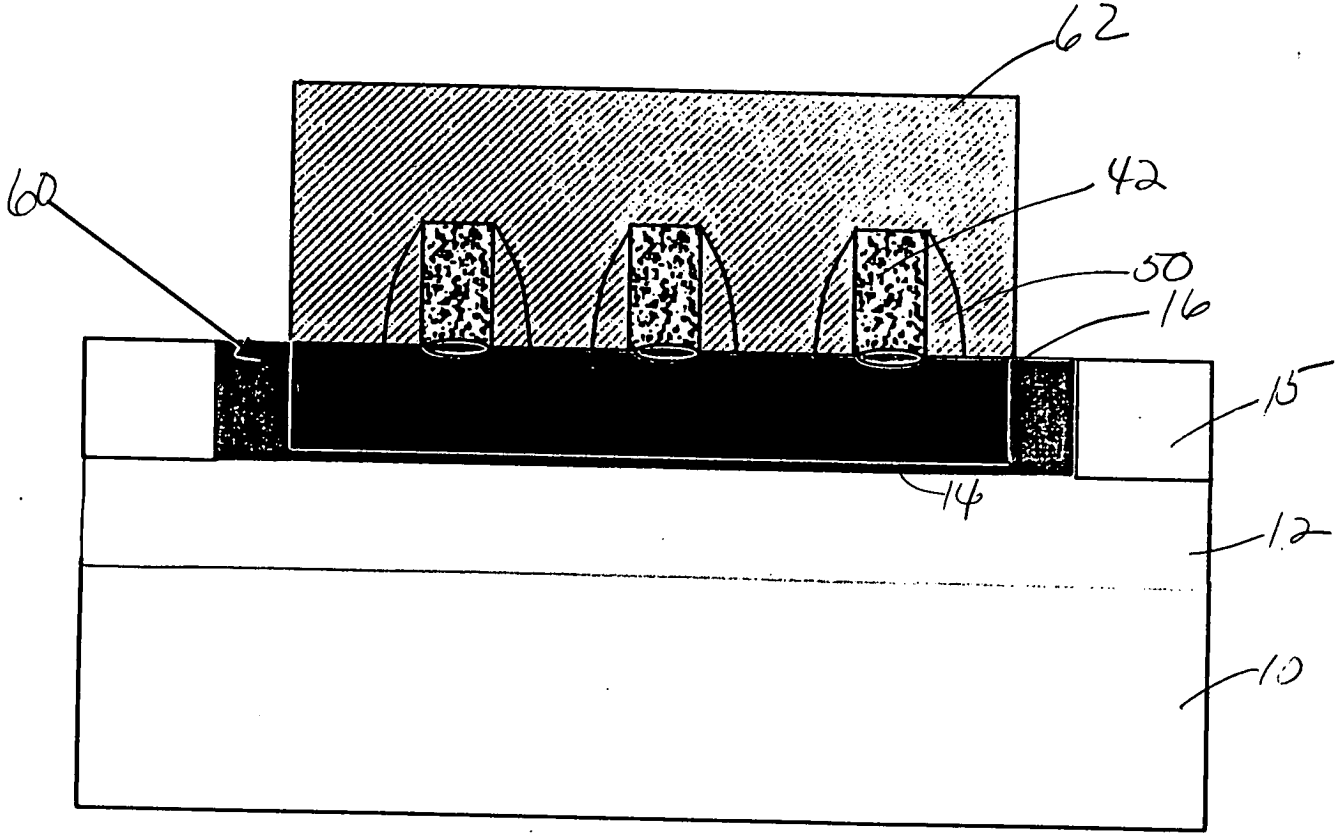


Figure 17

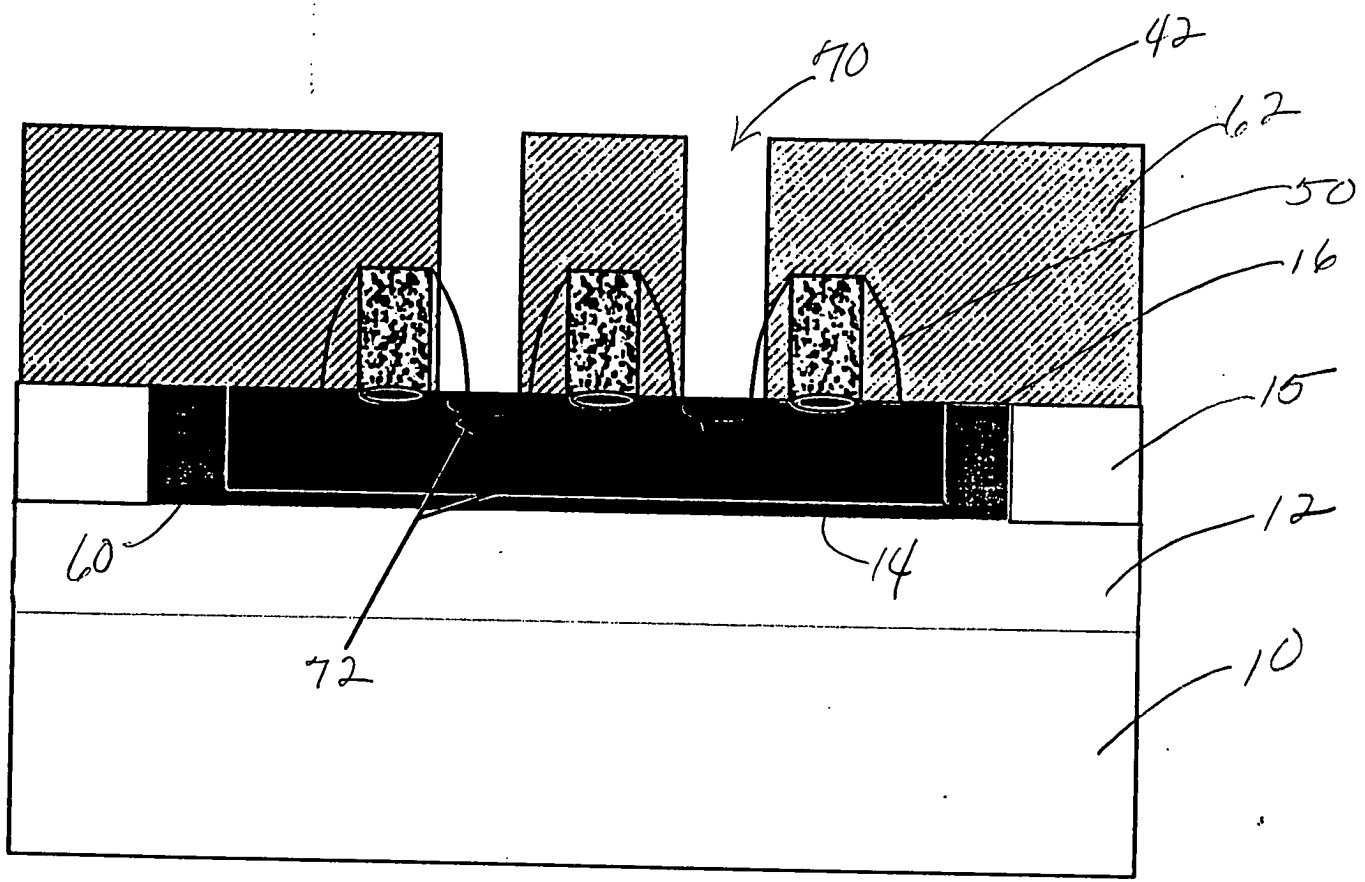


Figure 18

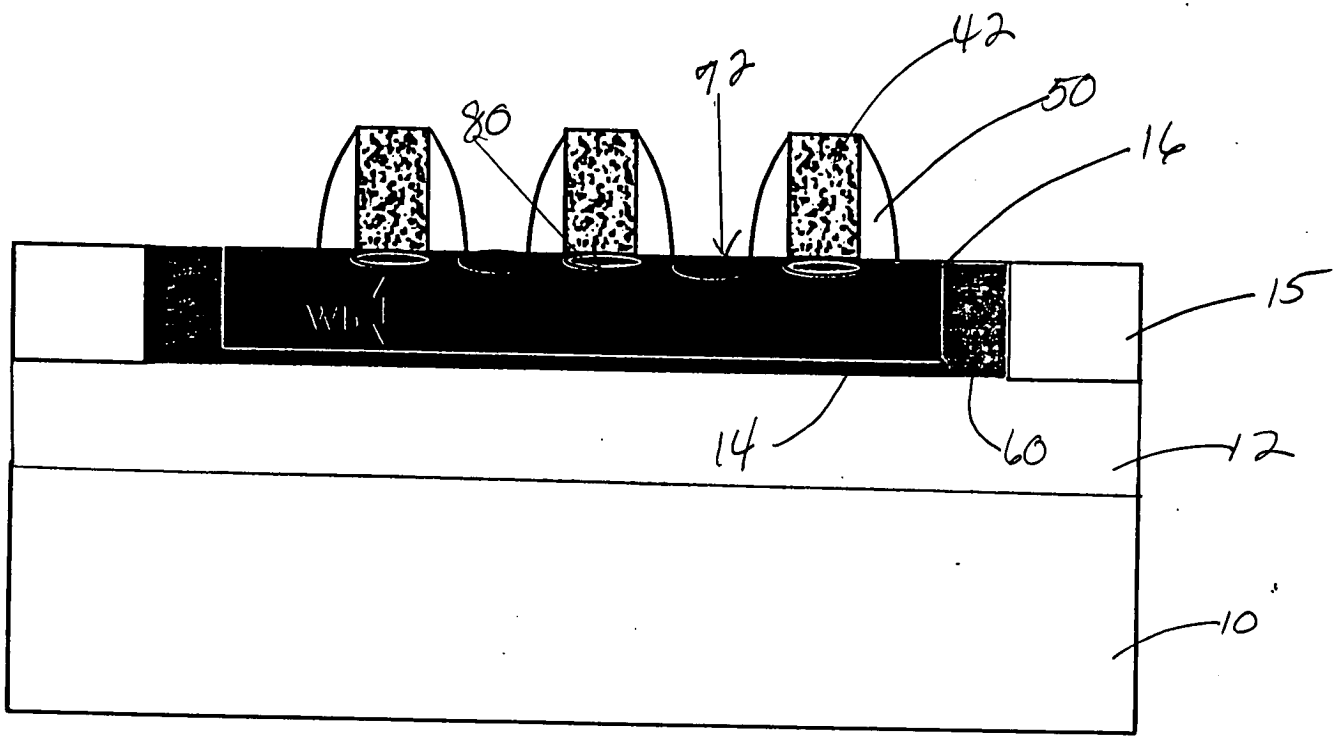
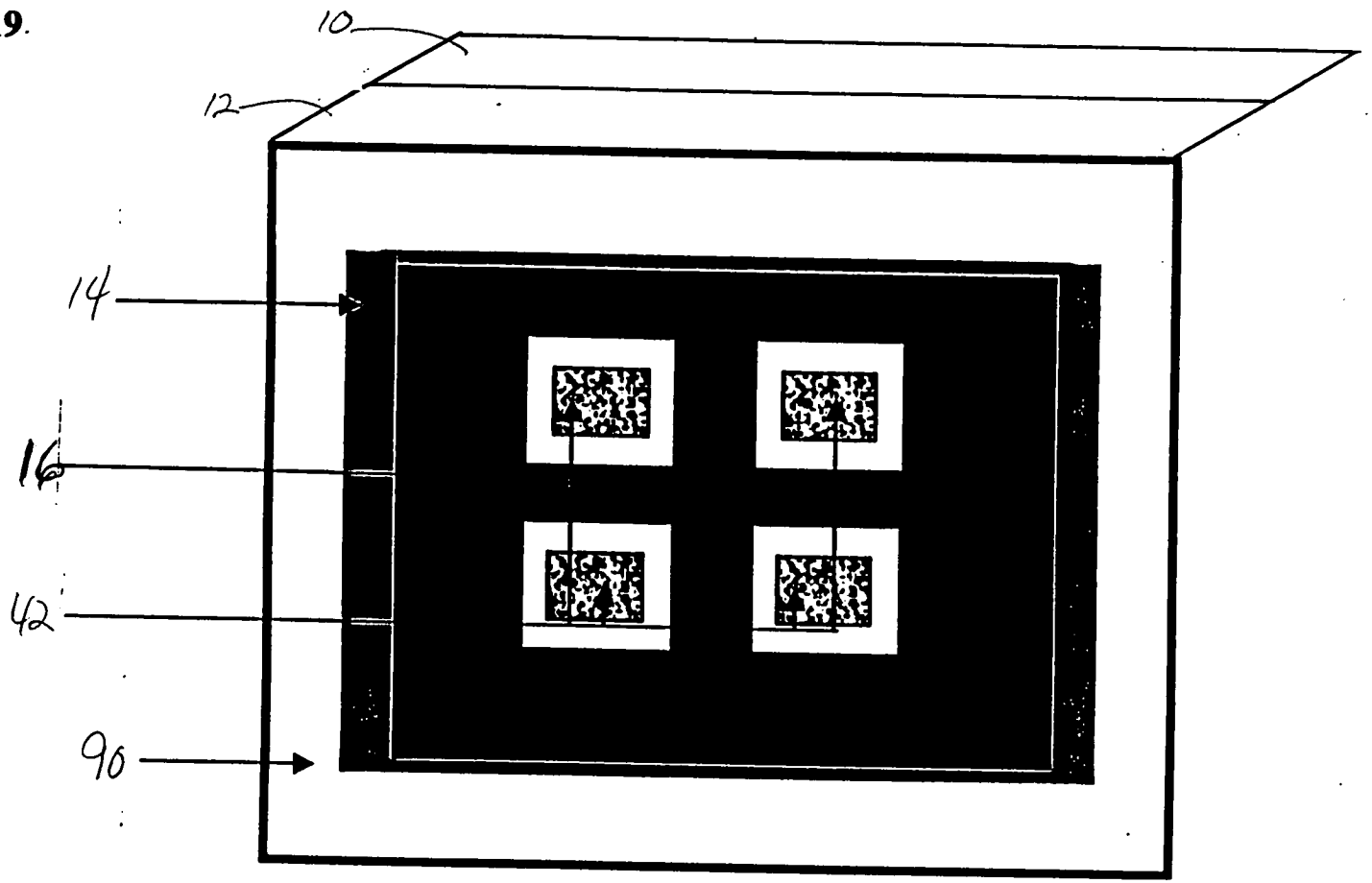


Figure 19.



Collector Doping Profile

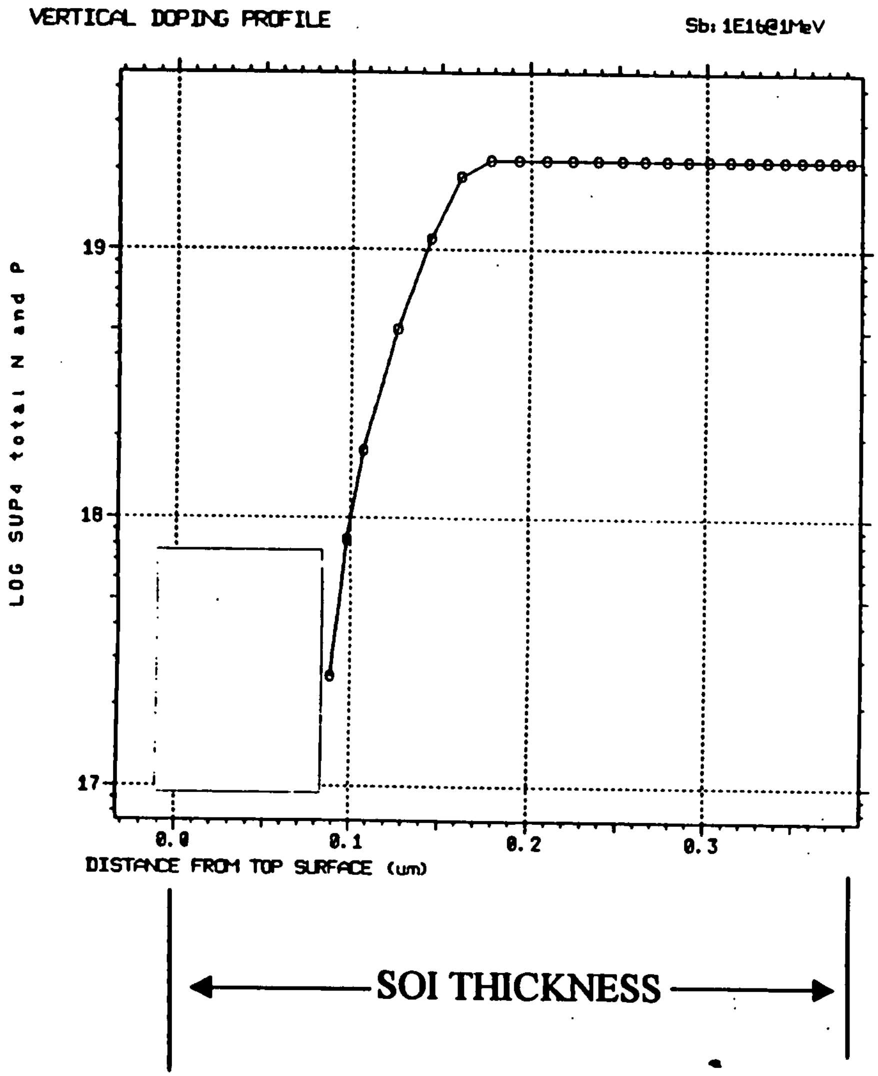


Figure 20H

D.C. Beta vs. Vbe

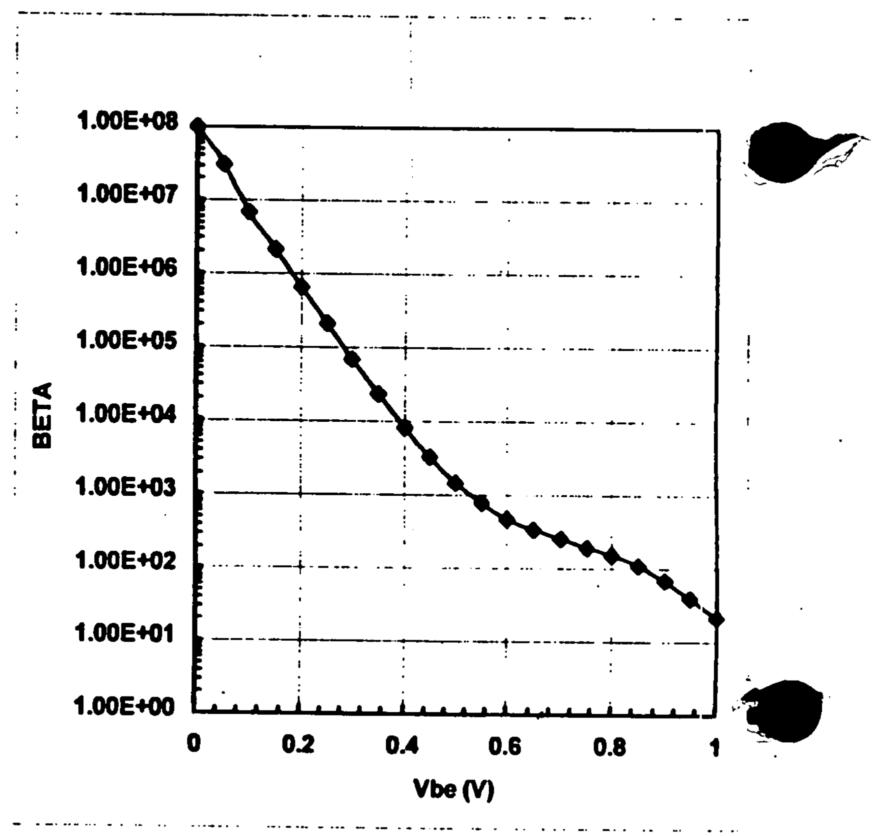


Figure 20B